WHAT IS CLAIMED IS:

1. A clock signal selector circuit, comprising:

a synchronizer circuit coupled to receive a first clock signal and a first control signal corresponding to the first clock signal, and configured to synchronize the first control signal to the first clock signal thereby producing a second control signal;

a first switching circuit coupled to receive the first clock signal and the second control signal, comprising an output terminal coupled to a first node, and configured to produce the first clock signal at the output terminal in the event the second control signal is asserted;

a multiplexer coupled between the first node and a second node and to receive the second control signal, and configured to drive the second node with a signal at the first node in the event the second control signal is asserted; and

a second switching circuit coupled between the first and second nodes and to receive the second control signal, and configured to form an electrical connection between the first and second nodes in the event the second control signal is deasserted.

2. The clock signal selector circuit as recited in claim 1, wherein the first switching circuit significantly reduces a probability of error at the second node due to metastability in the event the second control signal transitions from asserted to deasserted and the first clock signal is deselected.

3. The clock signal selector circuit as recited in claim 2, wherein in providing electrical feedback from the second node to the first node in the event the second control signal transitions from asserted to deasserted and the first clock signal is deselected, the second switching circuit further reduces the probability of error at the second node due to metastability.

4. The clock signal selector circuit as recited in claim 1, wherein the synchronizer circuit is coupled to receive a second clock signal and a third control signal corresponding to the second clock signal, and is configured to synchronize the third control signal to the second clock signal thereby producing a fourth control signal.

5. The clock signal selector circuit as recited in claim 4, wherein the multiplexer is coupled to a third node and to receive the fourth control signal, and configured to drive the second node with a signal at the third node in the event the fourth control signal is asserted.

6. The clock signal selector circuit as recited in claim 5, further comprising:

a third switching circuit coupled to receive the second clock signal and the fourth control signal, comprising an output terminal coupled to the third node, and configured to produce the second clock signal at the output terminal in the event the fourth control signal is asserted.

7. The clock signal selector circuit as recited in claim 6, further comprising:

a fourth switching circuit coupled between the second and third nodes and to receive the fourth control signal, and configured to form an electrical connection between the second and third nodes in the event the fourth control signal is deasserted.

8. The clock signal selector circuit as recited in claim 1, wherein the first switching circuit comprises a transmission gate or a tri-state buffer.

9. The clock signal selector circuit as recited in claim 1, wherein the first switching circuit comprises a first terminal coupled to receive the first clock signal, a second terminal coupled to the first node, and a control terminal coupled to receive the second control signal, and wherein the first switching circuit is configured to form an electrical connection between the first and second terminals in the event the second control signal is asserted.

10. The clock signal selector circuit as recited in claim 1, wherein the first switching circuit comprises a first terminal coupled to receive the first clock signal, a second terminal coupled to the first node, and a control terminal coupled to receive the second control signal, and wherein the first switching circuit is configured to drive the second terminal with the first clock signal in the event the second control signal is asserted.

11. The clock signal selector circuit as recited in claim 1, wherein the second switching circuit comprises a transmission gate or a tri-state buffer.

12. The clock signal selector circuit as recited in claim 1, wherein the second switching circuit comprises a first terminal coupled to the first node, a second terminal coupled to the second node, and a control terminal coupled to receive the second control signal, and wherein the second switching circuit is configured to form an electrical connection between the first and second terminals in the event the second control signal is deasserted.

13. The clock signal selector circuit as recited in claim 1, wherein the second switching circuit comprises a first terminal coupled to the first node, a second terminal coupled to the second node, and a control terminal coupled to receive the second control signal, and wherein the second switching circuit is configured to drive the first terminal with a signal at the second terminal in the event the second control signal is deasserted.

14. The clock signal selector circuit as recited in claim 1, further comprising:

a pair of storage elements connected in series between the second node and an output terminal of the clock signal selector circuit.

15. The clock signal selector circuit as recited in claim 14, wherein each of the pair of storage elements comprises a flip-flop.

16. A clock signal selector circuit, comprising:

a synchronizer circuit coupled to receive first and second clock signals and first and second control signals and configured to synchronize the first control signal to the first clock signal thereby producing a third control signal, and to synchronize the second control signal to the second clock signal thereby producing a fourth control signal;

a first switching circuit coupled to receive the first clock signal and the third control signal, comprising an output terminal coupled to a first node, and configured to produce the first clock signal at the output terminal in the event the third control signal is asserted;

a second switching circuit coupled to receive the second clock signal and the fourth control signal, comprising an output terminal coupled to a second node, and configured to produce the second clock signal at the output terminal in the event the fourth control signal is asserted;

a multiplexer coupled to the first and second nodes and to receive the third and fourth control signals, and comprising an output terminal coupled to a third node, and configured to drive the output terminal with a signal at the first node in the event the third control signal is asserted, and to drive the output terminal with a signal at the second node in the event the fourth control signal is asserted;

a third switching circuit coupled between the first and third nodes and to receive the third control signal, and configured to form an electrical connection between the first and third nodes in the event the third control signal is deasserted; and

a fourth switching circuit coupled between the second and third nodes and to receive the fourth control signal, and configured to form an electrical connection between the second and third nodes in the event the fourth control signal is deasserted.

17. The clock signal selector circuit as recited in claim 16, wherein the first and second switching circuits significantly reduce a probability of error at the third node due to metastability in the event the respective third and fourth control signals transition from asserted to deasserted and the respective first and second clock signals are deselected.

18. The clock signal selector circuit as recited in claim 17, wherein the third and fourth switching circuits further reduce the probability of error at the third node due to metastability by providing electrical feedback from the third node to the respective first and second nodes in the event the respective third and fourth control signals transition from asserted to deasserted and the respective first and second clock signals are deselected.

19. The clock signal selector circuit as recited in claim 16, wherein the first and second switching circuits comprise transmission gates or tri-state buffers, and wherein the third and fourth switching circuits comprise transmission gates or tri-state buffers.

20. The clock signal selector circuit as recited in claim 16, further comprising:

a pair of flip-flops connected in series between the third node and an output terminal of the clock signal selector circuit.